Schottky Bipolar 8214

PRIORITY INTERRUPT CONTROL UNIT

- Eight Priority Levels
- Current Status Register
- Priority Comparator
- Fully Expandable
- High Performance (50ns)
- 24-Pin Dual In-Line Package

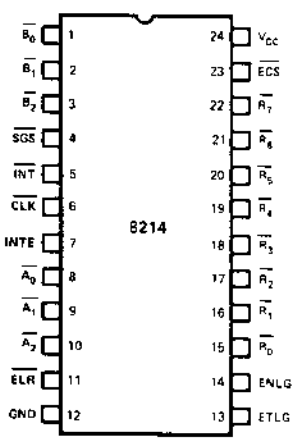
The 8214 is an eight level priority interrupt control unit designed to simplify interrupt driven microcomputer systems.

The PICU can accept eight requesting levels; determine the highest priority, compare this priority to a software controlled current status register and issue an interrupt to the system along with vector information to identify the service routine.

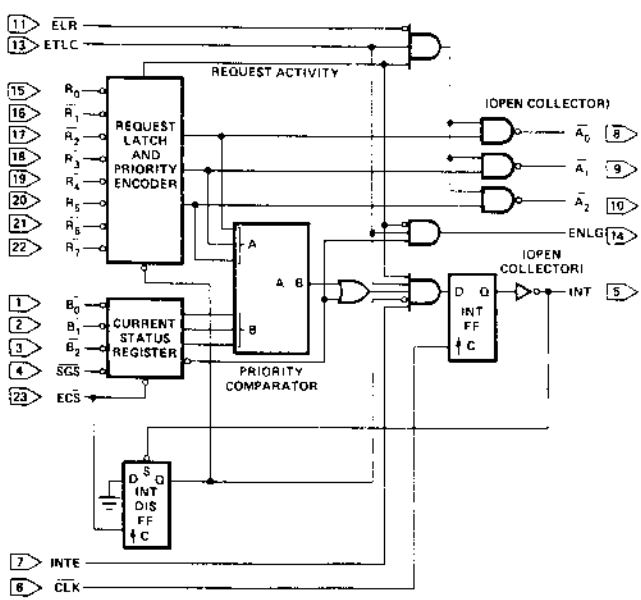
The 8214 is fully expandable by the use of open collector interrupt output and vector information. Control signals are also provided to simplify this function.

The PICU is designed to support a wide variety of vectored interrupt structures and reduce package count in interrupt driven microcomputer systems.

PIN CONFIGURATION



LOGIC DIAGRAM



PIN NAMES

INPUTS	
$\overline{R_0}$-$\overline{R_7}$	REQUEST LEVELS (R_7 HIGHEST PRIORITY)
$\overline{B_0}$-$\overline{B_2}$	CURRENT STATUS
$\overline{SGS}$	STATUS GROUP SELECT
$\overline{ECS}$	ENABLE CURRENT STATUS
INTE	INTERRUPT ENABLE
$\overline{CLK}$	CLOCK (INT F-F)
$\overline{ELR}$	ENABLE LEVEL READ
ETLG	ENABLE THIS LEVEL GROUP
OUTPUTS:	
$\overline{A_0}$-$\overline{A_2}$	REQUEST LEVELS — OPEN COLLECTOR
$\overline{INT}$	INTERRUPT (ACT LOW) — OPEN COLLECTOR
ENLG	ENABLE NEXT LEVEL GROUP

INTERRUPTS IN MICROCOMPUTER SYSTEMS

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient method so that large amounts of the total systems tasks can be assumed by the microcomputer with little or no effect on throughput.

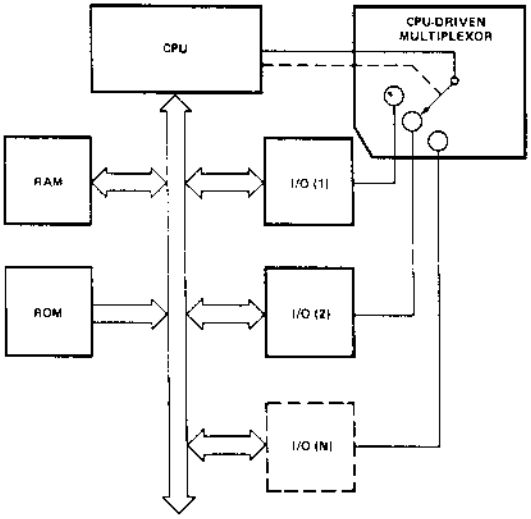
The most common method of servicing such devices is the **Polled** approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuence polling cycle and that such a method would have a serious, detrimental effect on system throughput thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desireable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete however the processor would resume exactly where it left off.

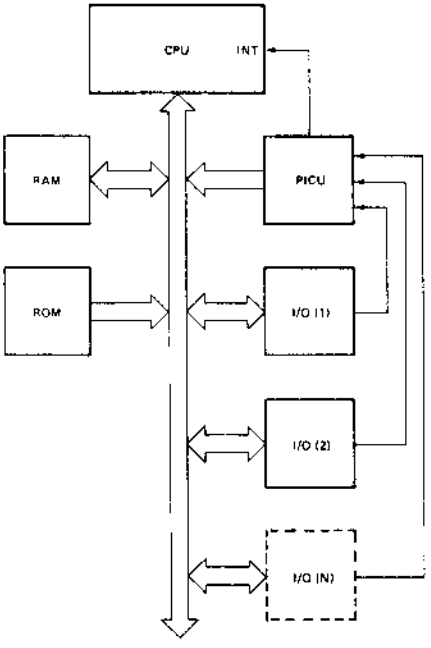
This method is called **Interrupt**. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Priority Interrupt Control Unit (PICU) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced and issues an Interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PICU, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. The PICU encodes the requesting level into such information for use as a "vector" to the correct Interrupt Service Routine.



Polled Method



Interrupt Method

FUNCTIONAL DESCRIPTION

General

The 8214 is a device specifically designed for use in real time, interrupt driven, microcomputer systems. Basically it is an eight (8) level priority control unit that can accept eight different interrupt requests, determine which has the highest priority, compare that level to a software maintained current status register and issue an interrupt to the system based on this comparison along with vector information to indicate the location of the service routine.

Priority Encoder

The eight requests inputs, which are active low, come into the Priority Encoder. This circuit determines which request input is the most important (highest priority) as preassigned by the designer. ($\overline{R7}$) is the highest priority input to the 8214 and ($\overline{R0}$) is the lowest. The logic of the Priority Encoder is such that if two or more input levels arrive at the same time then the input having the highest priority will take presidence and a three bit output, corresponding to the active level (modulo 8) will be sent out. The Priority Encoder also contains a latch to store the request input. This latch is controlled by the Interrupt Disable Flip-flop so that once an interrupt has been issued by the 8214 the request latch is no longer open. (Note that the latch does not store inactive requests. In order for a request to be monitored by the 8214 it must remain present until it has been serviced.)

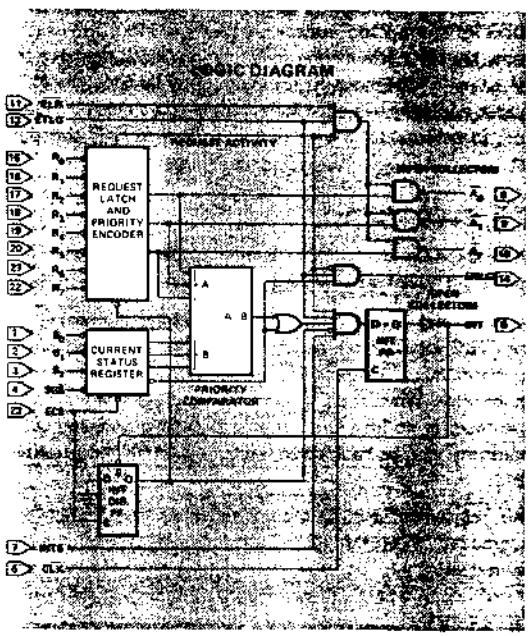
Current Status Register

In an interrupt driven microcomputer system it is important to not only prioritize incoming requests but to ascertain whether such a request is a higher priority than the interrupt currently being serviced.

The Current Status Register is a simple 4-bit latch that is treated as an addressable outport port by the microcomputer system. It is loaded when the $\overline{ECS}$ input goes low.

Maintenance of the Current Status Register is performed as a portion of the service routine. Basically, when an interrupt is issued to the system the programmer outputs a binary code (modulo 8) that is the compliment of the interrupt level. This value is stored in the Current Status Register and is compared to all further prioritized incoming requests by the Priority Comparator. In essence, a copy of the current interrupt level is written into the 8214 to be used as a reference for comparison. There is no restriction to this maintenance, other level values can be written into this register as references so that groups of interrupt requests may be disallowed under complete control of the programmer.

Note that the fourth bit in the register is $\overline{SGS}$. This input is part of the value written out by the programmer and performs a special function. The Priority Comparator will only issue an output that indicates the request level is greater than the Current Status Register. If both comparator inputs are equal to zero no output will be present. The $\overline{SGS}$ input allows the programmer to, in effect, disable this comparison and allow the 8214 to issue an interrupt to the system that is based only on the logic of the priority encoder.



Control Signals

The 8214 also has several inputs that enable the designer to synchronize the interrupt issued to the microprocessor and to allow or disallow such an issuance. Also, signals are provided that permit simple expansion to other 8214s so that more than eight levels can be controlled.

INTE, $\overline{CLK}$

The INTE (Interrupt Enable) input allows the designer to "shutoff" the interrupt system under control of external logic or possibly under software maintenance. A "zero" on this line will not allow interrupts to be issued to the microcomputer system.

The $\overline{CLK}$ (Clock) input is actually the trigger that strobes the Interrupt Flip-Flop. It can be connected to one of the clocks of the microprocessor so that the interrupt issued meets the CPU set-up time specification. Note that due to the gating of the input to the Interrupt Flip-Flop the $\overline{INT}$ output will only be active for the time of a single clock period, so external latching may be required to hold this signal.

$\overline{ELR}$, ETLG, ENGL

These three signals allow 8214s to be cascaded so that more than eight levels of interrupt requests can be controlled.

Basically, the ENLG output of one 8214 is connected to the ETLG input of the next and so on, with the first 8214 having its ETLG input pulled "high" and assigned the highest priority. When the ENLG output is "high" it indicates that there is no interrupt pending on that device and that interrupts can be monitored on the next lower priority 8214.

This "cascading" can be expanded almost indefinitely to accomodate even the largest of interrupt driven system architectures.

$\overline{A0}$, $\overline{A1}$, $\overline{A2}$

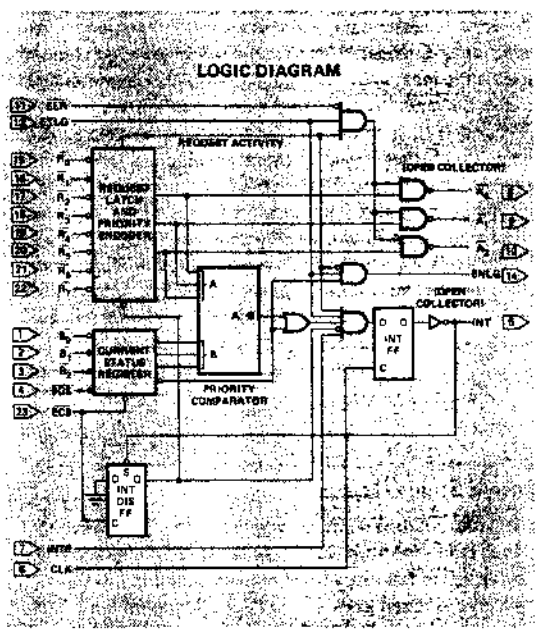
In order to identify which device has interrupted the processor so that the service routine associated with it can be addressed, a pointer or "vector" must accompany the interrupt issued to the microcomputer system.

The $\overline{A0}$, $\overline{A1}$ and $\overline{A2}$ outputs represent the complement of the active interrupt level (modulo 8). By using these signals to encode the special instruction, RST, the program counter of the microprocessor, can point to the location of the service routine. Note that these three outputs are gated by the $\overline{ELR}$ input and are open collector so that expansion is simplified.

$\overline{INT}$

The $\overline{INT}$ output of the 8214 is the signal that is issued to the microprocessor to initiate the interrupt sequence. As soon a $\overline{INT}$ is active the INT DIS FF is set, inhibiting further requests from entering the Request Latch. Only the writing out of the current status information by strobing the $\overline{ECS}$ input will clear the INT DIS FF and allow requests to enter the latch.

Note that $\overline{INT}$ is also open collector so that when cascaded to other 8214s an interrupt in any of the active devices will set all INT DIS FFs in the entire array.



APPLICATIONS OF THE 8214

8 Level Controller (8080)

The most common of applications of the 8214 is that of an eight level priority structure for 8080 or 8008 microcomputer systems.

Shown in the figure below is a detailed logic schematic of a simple circuit that will accept eight input requests, maintain current status, issue the interrupt signal to the 8080 and encode the proper RST instruction to gate onto the data bus.

The eight requests are connected to the 8214 by the designer in whatever order of priority is to be preassigned. For example, eight keyboards could be monitored and each assigned a degree of importance (level of priority) so that faster processor attention or access can be assigned to the critical or time dependent tasks.

The inputs to the Current Status Register are connected to the Data Bus so that data can be written out into this "port".

An 8212 is used to encode the RST instruction and also to act as a 3-state gate to place the proper RST instruction when the 8080 Data Bus is in the input mode. Note that the $\overline{INT}$ signal from the 8214 is latched in the SR flip-flop of the 8212 so that proper timing is maintained. The 8212 is selected (enabled) when the INTA signal from the 8080 status latch and the DBIN from the 8080 are active, this assures that the RST instruction will be placed on the Data Bus at the proper time. Note that the $\overline{INT}$ output from the 8212 is inverted and pulled up before it is connected to the 8080. This is to generate an $\overline{INT}$ signal to the 8080 that has the correct polarity and meets the input voltage requirement (3.3V).

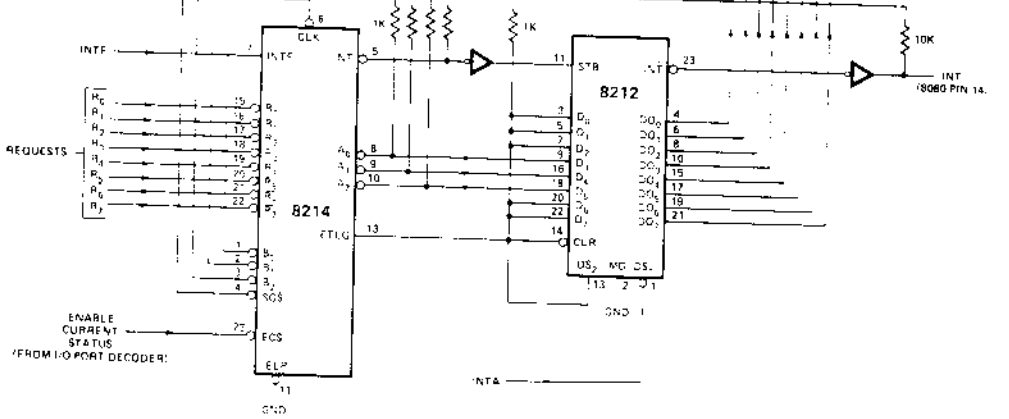
Basic Operation

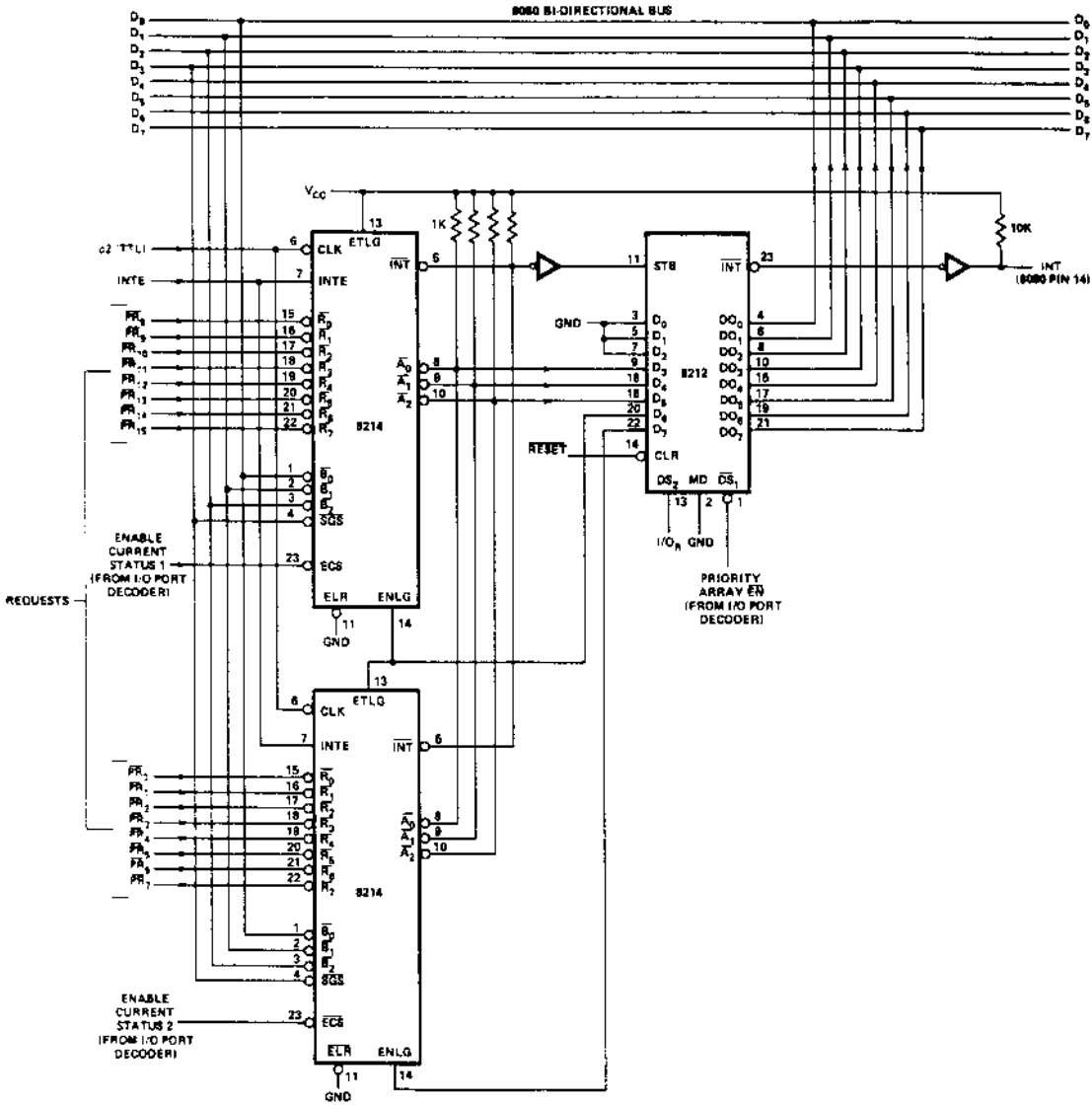
When the initial interrupt request is presented to the 8214 it will issue an interrupt to the 8080 if the structure is enabled. The 8214 will encode the request into 3 bits (modulo 8) and output them to the 8212. After the acknowledgement of the interrupt has been issued by the 8080 the encoded RST instruction is gated onto the Data Bus by the 8212. The processor executes the instruction and points the program counter to the desired serviced routine. In this routine the programmer will probably save the status of the register array and flags within a series of PUSH instructions (4). Then a copy of the current interrupt level (modulo 8) can be "built" in the Accumulator and output to the Current Status Register of the 8214 for use as a comparison reference for all further incoming requests to the system.

This Vectored Eight Level Priority Interrupt Structure for 8080 microcomputer systems is a powerful yet flexible circuit that is high performance and has a minimal component count.

PRIORITY (REQUEST)		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
	RST	1	1	A_2	A_1	A_0	1	1	1
LOWEST	0	1	1	1	1	1	1	1	1
	1	6	1	1	1	0	1	1	1
	2	5	1	1	0	1	1	1	1
	3	4	1	1	0	0	1	1	1
	4	3	1	0	1	1	1	1	1
	5	2	1	0	1	0	1	1	1
	6	1	1	0	0	1	1	1	1
HIGHEST	7	0	1	0	0	0	1	1	1

*RST 0 WILL VECTOR PROGRAM COUNTER TO LOCATION 0 (ZERO) AND INVOKE THE SAME ROUTINE AS "RESET" INPUT TO 8080
THIS COULD RE INITIALIZE THE SYSTEM BASED ON THE ROUTINE INVOKED
(A CAUTION TO SYSTEM PROGRAMMERS.)





16 Level Controller

APPLICATIONS OF THE 8214

Cascading the 8214

When greater than eight levels of interrupts must be prioritized and serviced, the 8214 can be cascaded with other 8214s to support such an architecture.

On the previous page a simple circuit is shown that can control 16 levels of interrupt and is easily expandable to support up to 40 levels of interrupt by just cascading more 8214s.

As described previously, there are signals provided in the 8214 for cascading ($\overline{ELR}$, ETLG, ENLG) and in effect the ENLG output of the first 8214 "ripples" down to the next and so on. The entire array of 8214s regardless of size, can be thought of as a single priority control unit, with the first having the highest priority and the next 8214 having a lower priority and so on.

In this application, the manner in which software handles the servicing of the interrupt will change. Since more than eight vectors must be generated a method other than the common RST instruction must be implemented. Basically, the priority control array must somehow modify the contents of the 8080 Program Counter so that it can point ("vector") to one of 16 (or how many levels are to be serviced) and fetch the proper service routine. A simple approach is to treat the priority control array as a single input port that can input a value into the Accumulator and use this value as an offset to modify the Program Counter (Indirect Jump).

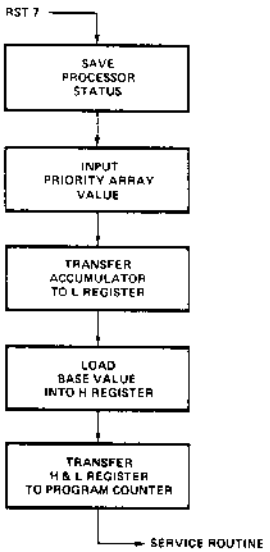
An initial CALL is needed to invoke this Indirect Jump routine so the circuitry is configured to insert an RST 7 (FFh) for all interrupts, thus the Indirect Jump Routine starts at location (56d).

The Assembly Code for the flow chart is as follows:

```
PUSH   PSW  ┐
PUSH   B    │
PUSH   D    ├  (save processor status)
PUSH   H    │  (22 microseconds)
            ┘
IN     (n)      (input Priority Array Value)
MOV    L,A      (transfer Accumulator to L register)
MVI    H,(n)    (load Base Address into H register)
PCHL            (transfer H&L to Program Counter)
```

(The execution time for the total routine is 35.5 microseconds based on an 8080 clock period of 500ns.)

Following is a basic flowchart of the priority array Indirect Jump routine. Note that the last step in the routine will vector the processor to fetch the proper service routine as dictated by the interrupting level.



REQUEST (PR) PRIORITIES		D_7 0-7 EN	D_6 8-15 EN	D_5 A_2	D_4 A_1	D_3 A_0	D_2 0	D_1 0	D_0 0
LOWEST	0	0	1	1	1	1	0	0	0
	1	0	1	1	1	0	0	0	0
	2	0	1	1	0	1	0	0	0
	3	0	1	1	0	0	0	0	0
	4	0	1	0	1	1	0	0	0
	5	0	1	0	1	0	0	0	0
	6	0	1	0	0	1	0	0	0
	7	0	1	0	0	0	0	0	0
	8	1	0	1	1	1	0	0	0
	9	1	0	1	1	0	0	0	0
	10	1	0	1	0	1	0	0	0
	11	1	0	1	0	0	0	0	0
	12	1	0	0	1	1	0	0	0
	13	1	0	0	1	0	0	0	0
	14	1	0	0	0	1	0	0	0
HIGHEST	15	1	0	0	0	0	0	0	0

Shown in the figure above is a chart of the 16 different array values that are used to offset the Program Counter and vector to the proper service routine. These values are the ones that are loaded into the "L" register; the value loaded into the "H" register with an "immediate instruction" is used to identify the major area of memory where the service routines are stored, similar to a "course setting" and the value in the "L" register is used to identify a specific location, similar to a "fine setting".

Note that D0, D1, and D2 are always set to "zero", this provides the programmer eight (8) memory locations between the start of each service routine so that maintenance of the associated Current Status Register and a JUMP or CALL instruction can be implemented.

This method of interrupt control can be almost indefinitely expanded and provides the system designer with a powerful tool to enhance total system throughput.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
All Output and Supply Voltages . . . . . -0.5V to +7V
All Input Voltages . . . . . -1.0V to +5.5V
Output Currents . . . . . 100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specifications is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

T_A = 0°C to +70°C, V_{CC} = 5V ±5%.

Symbol	Parameter		Limits			Unit	Conditions
			Min.	Typ.[1]	Max.		
V_C	Input Clamp Voltage (all inputs)				-1.0	V	I_C=-5mA
I_F	Input Forward Current:	ETLG input		-.15	-0.5	mA	V_F=0.45V
		all other inputs		-.08	-0.25	mA	
I_R	Input Reverse Current:	ETLG input			80	μA	V_R=5.25V
		all other inputs			40	μA	
V_{IL}	Input LOW Voltage:	all inputs			0.8	V	V_{CC}=5.0V
V_{IH}	Input HIGH Voltage:	all inputs	2.0			V	V_{CC}=5.0V
I_{CC}	Power Supply Current			90	130	mA	See Note 2.
V_{OL}	Output LOW Voltage:	all outputs		.3	.45	V	I_{OL}=15mA
V_{OH}	Output HIGH Voltage:	ENLG output	2.4	3.0		V	I_{OH}=-1mA
I_{OS}	Short Circuit Output Current:	ENLG output	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
I_{CEX}	Output Leakage Current:	$\overline{INT}$ and $\overline{A_0}$·$\overline{A_2}$			100	μA	V_{CEX}=5.25V

NOTES:
1. Typical values are for T_A = 25°C, V_{CC} = 5.0V.
2. B_0-B_2, $\overline{SGS}$, CLK, $\overline{R_0}$-$\overline{R_4}$ grounded, all other inputs and all outputs open.

A.C. CHARACTERISTICS AND WAVEFORMS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
t_{CY}	$\overline{CLK}$ Cycle Time	80	50		ns
t_{PW}	$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	25	15		ns
t_{ISS}	INTE Setup Time to $\overline{CLK}$	16	12		ns
t_{ISH}	INTE Hold Time after $\overline{CLK}$	20	10		ns
t_{ETCS}[2]	ETLG Setup Time to $\overline{CLK}$	25	12		ns
t_{ETCH}[2]	ETLG Hold Time After $\overline{CLK}$	20	10		ns
t_{ECCS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	80	50		ns
t_{ECCH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{ECRS}[3]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	110	70		ns
t_{ECRH}[3]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			
t_{ECSS}[2]	$\overline{ECS}$ Setup Time to $\overline{CLK}$	75	70		ns
t_{ECSH}[2]	$\overline{ECS}$ Hold Time After $\overline{CLK}$	0			ns
t_{DCS}[2]	$\overline{SGS}$ and $\overline{B_0}\cdot\overline{B_2}$ Setup Time to $\overline{CLK}$	70	50		ns
t_{DCH}[2]	$\overline{SGS}$ and $\overline{B_0}\cdot\overline{B_2}$ Hold Time After $\overline{CLK}$	0			ns
t_{RCS}[3]	$\overline{R_0}\cdot\overline{R_7}$ Setup Time to $\overline{CLK}$	90	55		ns
t_{RCH}[3]	$\overline{R_0}\cdot\overline{R_7}$ Hold Time After $\overline{CLK}$	0			ns
t_{ICS}	$\overline{INT}$ Setup Time to $\overline{CLK}$	55	35		ns
t_{CI}	$\overline{CLK}$ to $\overline{INT}$ Propagation Delay		15	25	ns
t_{RIS}[4]	$\overline{R_0}\cdot\overline{R_7}$ Setup Time to $\overline{INT}$	10	0		ns
t_{RIH}[4]	$\overline{R_0}\cdot\overline{R_7}$ Hold Time After $\overline{INT}$	35	20		ns
t_{RA}	$\overline{R_0}\cdot\overline{R_7}$ to $\overline{A_0}\cdot\overline{A_2}$ Propagation Delay		80	100	ns
t_{ELA}	$\overline{ELR}$ to $\overline{A_0}\cdot\overline{A_2}$ Propagation Delay		40	55	ns
t_{ECA}	$\overline{ECS}$ to $\overline{A_0}\cdot\overline{A_2}$ Propagation Delay		100	120	ns
t_{ETA}	ETLG to $\overline{A_0}\cdot\overline{A_2}$ Propagation Delay		35	70	ns
t_{DECS}[4]	$\overline{SGS}$ and $\overline{B_0}\cdot\overline{B_2}$ Setup Time to $\overline{ECS}$	15	10		ns
t_{DECH}[4]	$\overline{SGS}$ and $\overline{B_0}\cdot\overline{B_2}$ Hold Time After $\overline{ECS}$	15	10		ns
t_{REN}	$\overline{R_0}\cdot\overline{R_7}$ to ENLG Propagation Delay		45	70	ns
t_{ETEN}	ETLG to ENLG Propagation Delay		20	25	ns
t_{ECRN}	$\overline{ECS}$ to ENLG Propagation Delay		85	90	ns
t_{ECSN}	$\overline{ECS}$ to ENLG Propagation Delay		35	55	ns

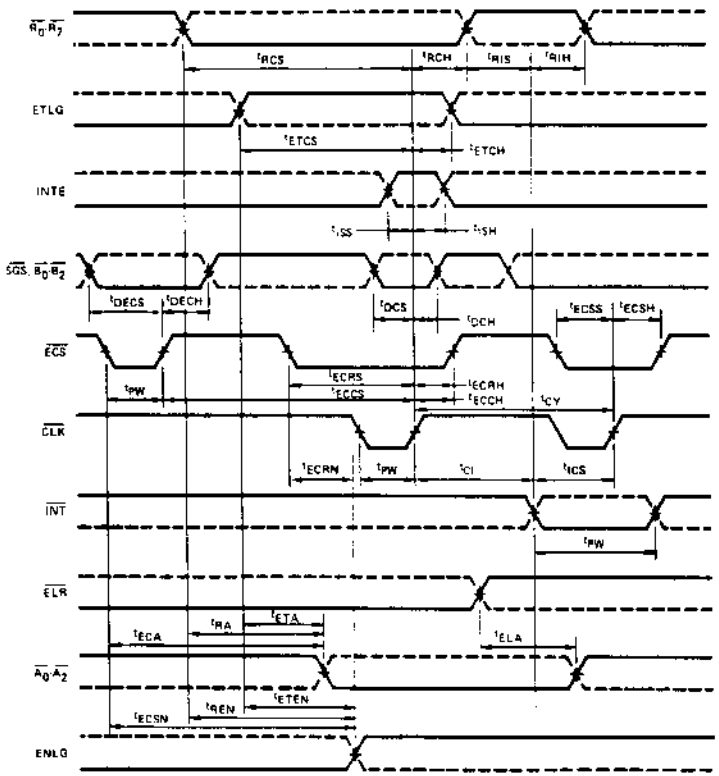
CAPACITANCE [5]

Symbol	Parameter	Limits Min.	Typ.[1]	Max	Unit
C_{IN}	Input Capacitance		5	10	pF
C_{OUT}	Output Capacitance		7	12	pF

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$, f = 1 MHz

NOTE 5. This parameter is periodically sampled and not 100% tested.

WAVEFORMS



NOTES:

(1) Typical values are for $T_A = 25°C$, $V_{CC} = 5.0V$.

(2) Required for proper operation if ISE is enabled during next clock pulse.

(3) These times are not required for proper operation but for desired change in interrupt flip-flop.

(4) Required for new request or status to be properly loaded.

TEST CONDITIONS:

Input pulse amplitude: 2.5 volts.

Input rise and fall times: 5 ns between 1 and 2 volts.

Output loading of 15 mA and 30 pf.

Speed measurements taken at the 1.5V levels.

TEST LOAD CIRCUIT